Price Indexes for Selected Semiconductors, 1974–96

By Bruce T. Grimm

IN THE comprehensive revision of the national income and product accounts (NIPA's) that was released in January 1996, BEA introduced the use of quality-adjusted price indexes for the calculation of real exports and imports of semiconductors. The improved measurement of real output and prices of high-tech goods through expanded use of quality-adjusted price indexes is part of BEA's strategic plan to improve the quality of its economic accounts (see the box "Measurement of Real Output and Prices for High-Tech Goods"). The quality-adjusted price indexes for semiconductors, which are based on indexes for several types of memory chips and of microprocessors, were incorporated into the estimates of exports and imports beginning with 1981.[1]

This article describes the development of quality-adjusted price indexes for seven types of metal oxide semiconductor (MOS) digital memory integrated circuits ("memory chips") and for two different lines of MOS digital microprocessor integrated circuits ("microprocessors"). It also describes the aggregation of the seven memory chip indexes into one summary index and the aggregation of the two microprocessor indexes into one summary index.

Memory chips, microprocessors, and other related integrated circuits are probably best known for their use in personal computers, but they can be found in a vast array of products, such as digital cable TV boxes, automobiles, and microwave ovens. In 1995, domestic shipments of memory chips were $11.1 billion, and domestic shipments of microprocessors were $11.4 billion. Most domestically produced memory chips and microprocessors are counted as intermediate consumption that is incorporated in the production of other goods. However, imports and exports of memory chips and microprocessors appear directly in estimates of GDP; in 1995, imports were $19.9 billion. and exports were $4.0 billion.

The new indexes described in this article use quality-adjusted prices in combination with Fisher chain-type indexes to produce price indexes for the 1974–96 period. These new indexes attempt to address biases associated with conventional measures of real output for high-tech products. As was noted in the most recent comprehensive NIPA revision, the introduction of these indexes resulted in a significantly faster rate of real growth of exports and imports. Among the more important results are the following:

- The price index for memory chips declined at a 37-percent average annual rate from 1975 to 1985 and at a 20-percent average annual rate from 1985 to 1996.
- The price index for microprocessors declined at a 35-percent average annual rate from 1985 to 1996.
- The price index for imports of semiconductors declined at a 19-percent average annual rate from 1985 to 1994; the previously used price index had increased at a 2-percent average annual rate. Reflecting this revision, real imports of semiconductors increased at a 47-percent average annual rate from 1985 to 1994; they had previously increased at a 17-percent average annual rate.
- The price index for exports of semiconductors declined at a 21-percent average annual rate from 1985 to 1994. The previously used price index had declined at a 2-percent average annual rate. Reflecting this revision, real exports of semiconductors increased at a 55-percent average annual rate from 1985 to 1994; they had previously increased at a 24-percent average annual rate.

The first section of this article examines the patterns of prices for memory chips and discusses the construction of price indexes for memory

1. See "Improved Estimates of The National Income and Product Accounts for 1959–95: Results of the Comprehensive Revision," SURVEY OF CURRENT BUSINESS 76 (January/February 1996): 27. The indexes also were incorporated into the improved estimates of gross domestic product by industry; see "Improved Estimates of Gross Domestic Product by Industry, 1959–94," SURVEY 76 (August 1996): 140–41. The indexes used in both of these sets of estimates were improved in the annual revision of the NIPA's that were released in July 1997; see "Annual Revision of the National Income and Product Accounts: Annual Estimates, 1993–96, and Quarterly Estimates, 1993:1-1997:1," SURVEY 77 (August 1997): 30.

chips based on prices per bit of memory. It also describes the results of hedonic regression experiments on two types of memory chips that examined how their performance characteristics determine their prices. The second section describes the characteristics of microprocessors and the results of hedonic regression experiments that examined how microprocessor prices are determined. It also describes how price indexes were constructed using both conventional methodologies and the hedonic regression results to support matched-model estimates. The third section describes how the summary price indexes for memory chips and microprocessors were used to construct price indexes that are used to deflate exports and imports of semiconductors and in the calculation of real gross product originating in the electronic and electronic equipment industry and in other industries.

The quality-adjusted price indexes for semiconductors cover 1974–96. BEA does not plan to extend its price estimates beyond 1996, because recent improvements by the Bureau of Labor Statistics in the methodologies used for estimating the producer price indexes for semiconductors make those indexes superior to those that can be generated using BEA's methodologies.

Data sources

Most of the price and quantity data that are used in this study were purchased from a commercial source.[2] In addition, some early-year price and quantity data for some types of memory chips were provided by Ellen Dulberger of the IBM Corporation. The data on the price-determining characteristics of both memory chips and mi-

2. The source was Dataquest, a subsidiary of the Gartner Group, Inc.

Measurement of Real Output and Prices for High-Tech Goods

The preparation of a new price index for semiconductors is part of a broader program that BEA has undertaken to improve its measures of the output and prices of high-tech goods in the national income and product accounts (NIPA's). These goods present problems for measurement because their quality and performance change rapidly and because their production costs and prices often fall relative to those of other goods. In particular, they pose problems for conventional fixed-weighted price indexes, for which the products in the sample and the relative weights are updated infrequently. Such indexes tend to miss the early part of a high-tech product's life cycle, when prices tend to decline rapidly, and to place too heavy a weight on the later part of the life cycle, when the prices of the older vintage technologies tend to decline less or even to rise.

Another measurement problem is the adjustment of prices for improvements in product quality. The conventional methodology assumes that an improvement in the quality of a product will be associated with an increase in the cost of producing it; the increase in cost is then used to determine how much of the product's price increase is attributable to quality difference and how much to pure price change. For high-tech goods, however, the cost and price of a new product—especially by the time it is beginning to replace an old product—are often lower than the old product.

BEA has attempted to improve its measures of output and prices through a combination of new weighting schemes and of new methods for assessing the impact of quality change. In 1995, BEA introduced chain-weighted price and quantity indexes that use a type of "superlative" index to address the bias associated with the use of fixed weights. These indexes use annual weights that reflect the adjustments that buyers make in purchasing patterns as relative prices change; thus, they more accurately measure overall changes in prices and in the pattern of production over time. However, these weights do not adjust for biases that arise from the use of fixed-weighted price indexes in the deflation of the detailed components of gross domestic product (GDP).[1]

BEA has attempted to address the problem of measuring quality change through the use of hedonic indexes and other quality adjustments. The hedonic indexes attempt to look explicitly at the differences in the prices and characteristics of high-tech and other products and to observe what consumers pay for various characteristics. Hedonic indexes were first used by BEA and IBM Corporation on a joint project to develop an improved price index for computers; this index was introduced into the NIPA's in 1986. This work has been largely taken over by the Bureau of Labor Statistics, which introduced hedonic price indexes for personal computers in 1990 and large-scale computers in 1997.

When BEA first introduced the computer price index, it was believed that the rapid decline in computer prices was partly due to declines in the prices of inputs, particularly of some types of semiconductors, to the computer manufacturing industry. However, the price indexes for semiconductors that were available showed only modest declines. If the prices of semiconductors were declining more rapidly than the price indexes indicated, the NIPA's were understating the increases in real imports and exports of semiconductors; in addition, real gross product would be overstated for the computer industry (in industrial machinery) and understated for the semiconductor industry (in electrical equipment). In researching this question, BEA, working with the Bureau of Labor Statistics, has developed several extensions of the earlier work on computer prices, including the quality-adjusted, reweighted price indexes for semiconductors that were introduced in the most recent comprehensive revision of the NIPA's and that are discussed in this article.

1. The Bureau of Labor Statistics (BLS) is examining the use of geometric means to address such lower level aggregation bias in the Consumer Price Index (CPI), components of which are used in deflating detailed components of consumer spending in GDP. BLS is not presently examining the use of geometric means in the Producer Price Index (PPI), components of which are used in deflating detailed components of investment and consumer spending in GDP. BLS believes that the PPI has a different conceptual basis than the CPI, and the use of geometric means is not "readily justifiable" within that conceptual framework. (See Bureau of Labor Statistics, "The Experimental CPI Using Geometric Means (CPI-U-XG)," April 10, 1997 at <http://www.bls.gov/cpigmrp.htm>.)

croprocessors came from both the commercial source and from published sources.

For memory chips, data on worldwide billing prices per unit and quantities of units shipped worldwide were used. These data cover a number of subtypes of memory chips, classified by chip "density," or the number of bits of data that can be stored on one chip. In addition, some types of memory chips have different capabilities: For example, DRAM chips are available in standard and video (VRAM) subtypes.

For microprocessors, the commercial-source data on North American booking prices—the prices at which orders are placed—and quantities of units shipped worldwide were used. These data cover a number of subtypes of microprocessors. For example, the price data on 80486 microprocessors includes six different subtypes that feature four different speeds of operation and three different configurations. Information from other published sources was used to identify the price-determining characteristics for each subtype of microprocessor. These characteristics are valued by the market, and differences in characteristics are reflected in the relative prices paid for the different types of microprocessors.

Beginning with 1974 for memory chips and 1985 for microprocessors, the data include prices and quantities only if there were significant numbers of shipments. Thus, the data set does not include early, limited shipments nor some late, limited shipments. In addition, only prices for the most prominent types of microprocessors are in the data set, and these are almost entirely from two manufacturers; microprocessors from "clone" suppliers are underrepresented in the data set. Nevertheless, the data set appears to cover most of the memory chips and microprocessors.

MOS Digital Memory Chips

Different types of memory chips have different performance characteristics and are typically used in different ways or in different types of products. As a result, the patterns of prices over time for the various types of chip are quite distinct. Due to the differing patterns, it was necessary to estimate separate price indexes for each type of chip.

Types of memory chips.—Quality-adjusted price indexes were estimated for seven types of memory chips:

DRAM Dynamic random access memory

EEPROM Erasable electronically programmable read-only memory

EPROM Electronically programmable read-only memory

Flash Flash memory; derived from EEPROM's

ROM Read-only memory

Fast SRAM Static random access memory, with access time of less than 70 nanoseconds

Slow SRAM SRAM with access time of more than 70 nanoseconds

Each type of memory chip is distinguished by its specific characteristics and uses.[3] For example, DRAM's are used for the main memories of personal computers, while SRAM's are generally used for their "cache" memories. Fast SRAM's command a higher price than slow SRAM's. Some additional data on price-determining technical characteristics are available for specific chip densities within chip types, and these chips are treated as separate subtypes. For example, DRAM chips that are specialized to speed computer video displays (VRAM technology) have been produced since the late 1980's, and these chips command a higher price than conventional DRAM's. The price indexes do not distinguish all the price-determining characteristics: According to Kenneth Flamm, chips with the same densities but with different configurations and packaging have different unit prices; however, the data do not contain enough information to make these distinctions.[4] Similarly, the data on DRAM's do not distinguish between parity and non-parity subtypes.

Life-cycle patterns.—Each chip density and subtype has a typical life-cycle pattern for prices and quantities. Quantities of shipments of chips of a specific density begin with small numbers, grow to a peak, and then decline to insignificant numbers. Unit prices start at typically high amounts, decline to a low, and then increase as the chip nears the end of its lifespan. The lows for unit prices may coincide with peak shipment rates, or they may lag several years. Table 1 illustrates this pattern for 16-kilobit DRAM's.

3. For more details about the various types of chips and their uses, see Winn L. Rosch, *The Winn L. Rosch Hardware Bible* (Indianapolis, IN: Sams Publishing, 1994):156–208.

4. See Kenneth Flamm, "Measurement of DRAM Prices: Technology and Market Structure," *Price Measurements and Their Uses*, ed. Murray Foss, Marilyn Manser, and Allan Young, (Chicago, IL: The University of Chicago Press, 1993): 157–197.

Prices per bit

For the selected chip types, the life-cycle price patterns for different chip densities result, over time, in chips with increasingly higher densities offering the lowest price per bit of storage capacity (table 2). This pattern starts with 4-kilobit DRAM chips in 1975 and ends with 16-megabit chips in 1995. In 1995, the cheapest price is less than 0.2 percent of the cheapest price in 1975.

Price indexes for the selected chip types.—The principal methodology used to estimate price indexes for the various chip types is an extension of Ellen Dulberger's work. It is a matched-model approach that is based on the unit prices and the density for each subtype of memory chip.[5] Separate indexes were estimated for each of the seven types of memory chips and were constructed using value weights derived from the price and quantity data.

Four annual price indexes were constructed for each type of memory chip. Three of the four are chain-type indexes that have weights that change each year: Price relatives for each density of each type of chip are weighted together, using the values of shipments, to obtain price indexes. The first index is a Laspeyres index that uses prior-year weights, the second is a Paasche index that uses current-year weights, and the third is a Fisher index, which is a superlative index that is constructed using the geometric average of the changes in the Laspeyres and Paasche indexes for each year.

The fourth index is calculated using the cheapest price per bit for any chip density in each year. This index provides a rough proxy for changes in the cost of the cheapest available technology for products that are designed to minimize cost and that require the amount of memory provided by the cheapest price-per-bit chip. This index is used only to provide a rough check on the price changes found using the other three indexes. In order for this index to be the useful in estimating quality-adjusted price indexes, the other characteristics of chip subtypes—which are not accounted for in this price index—would have to be unimportant, contrary to the price differentials reported by Flamm.

Table 3 shows the average rates of change for the four indexes for 1977–96. It was possible to construct all four indexes for five of the memory chip types: The declines in the indexes based on the "cheapest" price per bit are generally of the same order of magnitude as those in other indexes, but they are the largest for four of the five chip types. The declines in the Fisher indexes vary from 18 percent for EEPROM's to 31 percent for DRAM's. The Fisher index for Flash memory chips declines at a 37-percent rate for the shorter period for which that index is available.[6]

The pattern of memory chip prices.—In order to summarize the changes in quality-adjusted price indexes for memory chips over time, a Fisher chain-type index was constructed using the Fisher price indexes for the seven individual

5. See Ellen Dulberger, "Sources of Price Decline in Computer Processors: Selected Electronic Components," in *Price Measurements and Their Uses*, ed. Murray Foss, Marilyn Manser, and Allan Young (Chicago, IL: The University of Chicago Press, 1993) 103–124.

6. Some indexes for EEPROM's and ROM's are not shown because the estimates before 1988 were based on Dulberger's data. The methodology used to link the estimates based on Dulberger's data with the other estimates does not support the calculation of these indexes.

Table 1.—Prices and Quantities Shipped of 16 Kilobit DRAM's

Year	Dollars	Thousands
1976	52.50	54
1977	23.00	2,008
1978	9.25	20,785
1979	6.13	53,218
1980	4.81	184,020
1981	2.11	221,473
1982	1.24	286,290
1983	1.05	296,610
1984	1.11	161,290
1985	1.34	70,920
1986	.....	.....

DRAM Dynamic random access memory

Table 2.—DRAM Prices

[Dollars per kilobit]

Chip type	1975	1980	1985	1990	1995
4 kilobit	***1.8125***	0.4813	0.9375	.....	.....
16 kilobit	.....	***0.3008***	0.0836	.....	.....
64 kilobit	.....	0.9766	***0.0170***	0.0226	0.0188
256 kilobit	.....	.....	0.0194	0.0077	0.0078
1 megabit	.....	.....	0.1184	***0.0061***	0.0039
4 megabit	.....	.....	.....	0.0103	0.0031
16 megabit	.....	.....	.....	.....	***0.0030***

NOTE.—Bold italics indicate lowest price per bit of memory for the corresponding year.
DRAM Dynamic random access memory (standard technology)

Table 3.—Price Indexes: Average Annual Rates of Change, 1977–96

[Percent]

Chip type	Fisher chain	Laspeyres chain	Paasche chain	Cheapest
DRAM's	–31.1	–28.2	–34.0	–28.7
EEPROM's	–17.8	.....	.....	.....
EPROM's	–27.8	–27.9	–28.0	–32.3
Flash (1988–96)	–37.4	–39.3	–35.4	–40.1
ROM's	–21.7	.....	.....	.....
Fast SRAM's	–26.7	–27.3	–25.2	–28.6
Slow SRAM's	–19.9	–21.2	–18.5	–28.3

DRAM Dynamic random access memory
EEPROM Erasable electronically programmable read-only memory
EPROM Electronically programmable read-only memory
Flash Flash memory
ROM Read-only memory
SRAM Static random access memory

memory chip types as the components (table 4). This index reflects both the price indexes for the individual chip types and their changing value weights: In particular, note that the weight for DRAM's increased from about one-third of the total in the early 1980's to about two-thirds in 1995–96.

The index declines sharply in most years in 1975–92. However, the index declines more slowly in 1987 and then increases in 1988, reflecting the xffects of the U.S.-Japan Semiconductor Trade Agreement in late 1986.[7] In 1993, the decline in the index slows, and in 1994, the index increases slightly. It declines modestly in 1995 and very rapidly in 1996, as overcapacity in worldwide chip-production facilities led to sharp price cuts in DRAM's, beginning in the first quarter of 1996.

Fisher chain-type price indexes for each type of memory chip are shown in table 5. The time patterns for the indexes are roughly similar to those of the summary index. The indexes for DRAM's and fast SRAM's generally decline more rapidly than the other indexes, and the indexes for ROM's and slow SRAM's generally decline more slowly. These patterns support Dulberger's finding that the prices of the various types of MOS memory chips declined sharply from the mid-1970's through the mid-1980's.[8] They also indicate continuing sharp declines through 1992. In 1993, however, the declines generally slowed or halted, and prices of several types of memory chips increased in 1994. In 1995 and 1996, the prices of nearly all types of memory chips declined.

Table 4.—Summary Price Index for Memory Chips

[1992=1.00]

Year	Index	Percent change from previous year
1974	1,778.37	.....
1975	560.57	–68.5
1976	343.62	–38.7
1977	199.23	–42.0
1978	116.68	–41.4
1979	97.33	–16.6
1980	68.97	–29.1
1981	33.48	–51.4
1982	20.73	–38.1
1983	15.13	–27.0
1984	11.86	–21.6
1985	5.57	–53.0
1986	3.61	–35.2
1987	3.23	–8.0
1988	3.87	16.5
1989	3.29	–15.1
1990	1.83	–44.5
1991	1.30	–29.0
1992	1.00	–22.4
1993	0.94	–6.4
1994	0.94	0.3
1995	0.87	–7.6
1996	0.47	–46.0
Averages:		
1975–85	.....	–36.9
1985–96	.....	–20.1

Regression experiments

The prices of memory chips are determined by several factors, or quality characteristics. Hedonic regressions may be used to estimate the values

7. See Flamm, 163–64.

8. See Dulberger, 115–18.

Table 5.—Price Indexes for MOS Memory Chips

[1992=1.00]

Year	DRAM's		EEPROM's		EPROM's		Flash memories		ROM's		Fast SRAM's		Slow SRAM's	
	Index	Percent change from previous year	Index	Percent change from previous year	Index	Percent change from previous year	Index	Percent change from previous year	Index	Percent change from previous year	Index	Percent change from previous year	Index	Percent change from previous year
1974	4,173.40	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....
1975	1,315.53	–68.5	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	129.52	.....
1976	805.19	–38.8	.....	.....	726.08	.....	.....	.....	.....	.....	.....	.....	81.31	–37.2
1977	480.58	–40.3	24.42	.....	374.35	–48.4	.....	.....	74.99	.....	125.84	.....	46.60	–42.7
1978	267.55	–44.3	18.07	–26.0	163.21	–56.4	.....	.....	45.62	–39.2	95.69	–24.0	36.91	–20.8
1979	215.35	–19.5	13.40	–25.9	131.49	–19.4	.....	.....	40.93	–10.3	85.21	–11.0	31.72	–14.1
1980	175.99	–18.3	10.97	–18.1	71.49	–45.6	.....	.....	31.13	–23.9	41.29	–51.5	23.49	–26.0
1981	75.32	–57.2	9.45	–13.8	24.30	–66.0	.....	.....	21.60	–30.6	19.79	–52.1	12.49	–46.8
1982	38.25	–49.2	8.80	–6.9	16.10	–33.7	.....	.....	15.82	–26.7	11.38	–42.5	7.51	–39.9
1983	27.58	–27.9	8.54	–3.0	11.47	–28.7	.....	.....	10.83	–31.5	10.59	–6.9	5.70	–24.1
1984	21.57	–21.8	7.41	–13.1	8.24	–28.2	.....	.....	8.82	–18.6	10.85	2.4	4.79	–16.0
1985	7.39	–65.7	5.08	–31.5	4.28	–48.0	.....	.....	5.44	–38.3	7.49	–30.9	2.83	–40.9
1986	4.34	–41.3	3.82	–24.8	2.94	–31.3	.....	.....	3.98	–27.0	5.00	–33.3	1.97	–30.2
1987	3.99	–8.0	3.36	–12.0	3.04	3.4	.....	.....	3.08	–22.7	3.95	–21.0	1.82	–8.0
1988	5.08	27.3	2.69	–19.9	3.19	5.0	10.92	.....	2.00	–35.1	3.92	–0.8	2.62	44.2
1989	4.43	–12.8	2.30	–14.7	2.29	–28.2	5.46	–50.0	1.57	–21.6	3.43	–12.5	2.41	–7.8
1990	2.14	–51.8	1.73	–24.9	1.43	–37.8	2.08	–61.8	1.29	–17.8	2.19	–36.1	1.38	–42.8
1991	1.42	–33.5	1.23	–28.7	1.13	–21.0	1.20	–42.3	1.07	–16.6	1.42	–34.9	1.10	–20.3
1992	1.00	–29.5	1.00	–18.7	1.00	–11.2	1.00	–16.8	1.00	–6.8	1.00	–29.8	1.00	–9.1
1993	0.98	–1.5	0.92	–8.2	0.88	–12.1	0.88	–12.3	0.77	–22.5	0.66	–33.6	1.03	2.7
1994	1.01	2.2	0.74	–19.7	0.88	0.7	0.63	–28.3	0.84	7.8	0.62	–6.3	1.01	–2.0
1995	0.98	–2.6	0.62	–16.2	0.74	–16.9	0.38	–39.9	0.77	–8.2	0.40	–36.0	0.82	–19.0
1996	0.40	–59.4	0.59	–4.2	0.76	3.4	0.26	–32.0	0.71	–7.3	0.35	–13.3	0.69	–15.5

DRAM Dynamic random access memory
EEPROM Erasable electronically programable read-only memory
EPROM Electronically programmable read-only memory
Flash Flash memory
MOS Metal oxide semiconductor
ROM Read-only memory
SRAM Static random access memory

of the quality characteristics.[9] In order to evaluate the possible usefulness of hedonic regressions for supporting the estimation of quality-adjusted price indexes for memory chips, regressions were estimated for two types of chips—DRAM's and EPROM's. DRAM's were chosen because of their large share in total memory chip shipments, and EPROM's were chosen to evaluate whether the results from the regressions for DRAM's tended to hold for other types of memory chips. In addition, both types of memory chips were chosen because they have been produced for a relatively long time. Together, DRAM's and EPROM's accounted for two-thirds of the commercial-source data's estimates of the value of worldwide shipments of MOS digital memory integrated circuits in 1980 and for more than three-quarters in 1994.

The determinants of memory chip prices.—Only limited information about the characteristics of DRAM's and EPROM's is available, including annual data for worldwide unit prices for shipments, chip density, and quantities shipped. In addition, it is possible to construct measures of how long the chips of each density had been produced in significant numbers and of the ratio of their density to that of the cheapest per-bit density of chip.

As noted earlier, Kenneth Flamm found that other chip characteristics, such as packaging and the way that the memory is grouped on the chip are also significant in determining unit prices.[10] However, data on these characteristics were not available.

The primary explanatory variable is density. By and large, it is expected that larger capacity, higher density memory chips will sell for more than lower density chips. An examination of the data on prices largely confirms this. However, some types of older memory chips have higher unit prices than newer, higher density memory chips, but the quantities of shipments of these older chips are usually small.

A second explanatory variable may be a general decline in memory chip prices over time. This tendency is evident in the pronounced downtrend in the summary Fisher chain-type price index.

An additional factor for DRAM's is the appearance in the mid-1980's of VRAM technology chips, which led to persistent price premiums for VRAM's. The prices of VRAM chips have been roughly double the prices of standard technology DRAM chips of the same density.

The U.S.-Japan Semiconductor Trade Arrangement in late 1986 led temporarily to higher unit prices for some types of memory chips. To account for the effects of the arrangement on chip prices, experiments were performed with dummy variables. The effects were statistically significant for both chip types in 1988 and for DRAM's in 1989, but they were not statistically significant for 1987 or for years after 1989.[11] For both types of chips, the preferred equations used a dummy variable with a value of 1 in 1988 and 1989 and a value of zero elsewhere.

The price patterns for DRAM's appear to follow the typical life cycle (chart 1).[12] The unit prices are initially very high, then decline—rapidly at first and then less rapidly—to reach a low range, and finally tend to increase until significant shipments end. However, most densities of DRAM's are still being shipped.

9. Hedonic regressions have been used by BEA to support the estimation of quality-adjusted price indexes for mainframe and personal computers. For a discussion of the use of hedonic regressions to estimate price indexes for mainframe computers, see Roseanne Cole, Y. C. Chen, Joan A. Barquin-Stolleman, Ellen Dulberger, Nurhan Helvacian, and James H. Hodge, "Quality-Adjusted Price Indexes for Computer Processors and Selected Peripheral Equipment," SURVEY OF CURRENT BUSINESS 66 (January 1986): 41–50. For a discussion of the use of hedonic techniques for estimating price indexes, see Jack E. Triplett, "The Economic Interpretation of Hedonic Methods," SURVEY 66 (January 1986): 36–40.

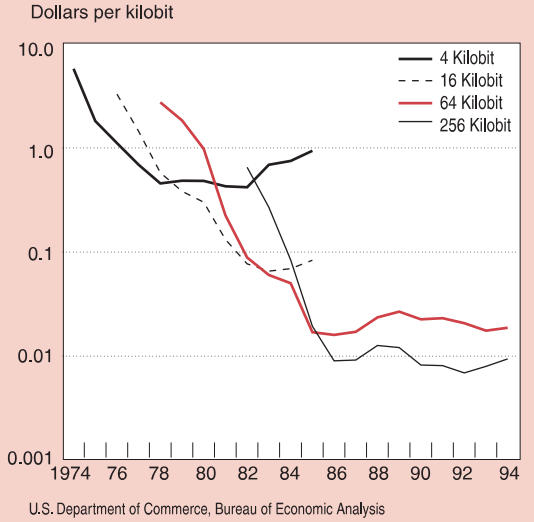
10. See Flamm, 158–161.

11. Experiments were also performed with individual-year time dummy variables in an attempt to find time-related price declines that were not captured elsewhere in the equation for DRAM prices, but these efforts were unsuccessful.

12. Ellen Dulberger suggested the existence of a life-cycle pattern in an informal discussion with BEA staff.

CHART 1

DRAM Prices Per Bit of Memory



U.S. Department of Commerce, Bureau of Economic Analysis

This life-cycle pattern also appears to apply to other types of memory chips. The early price declines probably reflect a learning curve for the manufacturers, economies of scale, and increasing competition as more manufacturers supply the memory chips. The later price increases appear to reflect decreasing economies of scale and declining competition as fewer manufacturers supply the memory chips. It seems likely that the life-cycle pattern is primarily a result of supply and not demand; if so, then variables explaining the life cycles should not be used in estimating hedonic price indexes.

Two proxy variables were constructed to account for life-cycle patterns. The first is a nonlinear variable based on how long memory chips of a given type and density have been shipped. This variable is designed to decrease rapidly at first and then less rapidly to reach a low, constant value at 7 years, the typical time for a chip's price to reach the low range. The functional form chosen was

$$\text{Nlage7max} = (8 - \min(\text{age},7))^2,$$

where *age* is the number of years that shipments of the memory chip's density and type are recorded. For example, the age of 16-kilobit DRAM's, which were first shipped in significant numbers in 1976, in 1979 was 3.

The second proxy variable is the ratio of each chip's density to the density of the cheapest price-per-bit chip of the same type. Because the cheapest per-bit chips have had increasingly higher densities over time and because lower density chips are those whose prices tend to increase, this variable proxies for the price increases. This variable also helps to explain the initial price declines because new, higher density chips are those whose prices tend to decline and because they have large ratios of own densities to those of the cheapest price-per-bit chips.

Four functional forms were used in the initial regression experiments: Log-log, log-linear, linear-linear, and linear-log. Log-log and log-linear forms were clearly superior, and only equations with these two forms are shown.

The sample period used is 1976–94. The earliest data for EPROM's is for 1976, so it was chosen as the initial year in equations for both types of memory chips for the sake of uniformity. The year 1994 was the latest year for which data were available at the time the regressions were estimated. The sample period was not extended, because new technical characteristics emerged—in particular, "fast page mode" and "extended data out" technologies for DRAM's—that affected memory chip prices in ways that could not be captured by the available data on explanatory variables.

Results of regression equations.—The results for selected equations for the logarithm of unit prices for DRAM's are shown in table 6. The explanatory variables are as follows:

Density Number of bits of data that may be stored on a chip, in kilobits

Time Year of the price observation (for example, 1976 = 76)

Stan-vram Dummy variable for VRAM technology; standard DRAM technology = 0, VRAM technology = 1

Nlage7max Nonlinear variable for the age of the chip's density class, as described earlier

Cheaprat Ratio of the chip's density to the density of the cheapest per-bit chip (for example 64K/1M = 0.0625)

Dum8889 Dummy variable for the effects of the semiconductor trade agreement; 1988–89 = 1, other years = 0

Equation 1 uses the logarithm of density and a linear time trend as explanatory variables. Both explanatory variables are highly significant statistically. Equation 2 adds the two variables that explain the life-cycle patterns of prices for individual chip densities and the dummy variable for VRAM technology. The measure of the time trend was changed to a logarithmic one in order to keep time as a statistically significant explanatory variable. The equation has an improved fit,

Table 6.—Hedonic Regressions for DRAM's, 1976–94

[Coefficients, with t-test statistics in parentheses]

Explanatory variable	Equation number				
	1	2	3	4	5
Density	.....	.....	0.00040	0.00038	0.00038
	.....	.....	(7.92)	(10.03)	(10.32)
Log (Density)	0.88575	0.32690	.....	.....	.....
	(14.32)	(4.83)	.....	.....	.....
Time	–0.27168	.....	–0.00702	.....	.....
	(10.49)	.....	(0.51)	.....	.....
Log (Time)	.....	–4.72498	.....	.....	.....
	.....	(1.99)	.....	.....	.....
Stan-vram	.....	0.78798	1.01305	0.99964	0.95543
	.....	(4.68)	(7.29)	(7.41)	(7.19)
Nlage7max	.....	0.04630	0.04947	0.05023	0.05412
	.....	(9.08)	(13.27)	(14.81)	(15.30)
Cheaprat	.....	0.05285	0.06563	0.06617	0.05369
	.....	(2.40)	(3.61)	(3.67)	(2.90)
Dum8889	.....	.....	.....	.....	0.33529
	.....	.....	.....	.....	(2.21)
Constant	21.0254	20.2759	0.99367	0.38423	0.35181
	(10.35)	(1.96)	(0.82)	(5.04)	(4.63)
R-bar square	0.6956	0.8680	0.9035	0.9043	0.9085
F-test statistic	102.68	118.59	167.59	211.28	177.76
	(2,87)	(5,84)	(5,84)	(4,85)	(5,84)

NOTE.—The dependent variable is the natural logarithm of the unit price of a DRAM.
DRAM Dynamic random access memory

as measured both by R-bar square and the F-test statistic.

Equation 3 substitutes the level of density for its logarithm. With this specification, both forms of the time trend continue to have negative coefficients, but are insignificant. Deleting the time trend yields equation 4, which is otherwise similar to equation 3. The coefficients for the nontime explanatory variables all continue to be highly significant.

Equation 5 adds the variable for the semiconductor trade agreement. It is positive, as expected, and is statistically significant at the 0.95 confidence level. The values of the statistic for the F-test and R-bar square are highest for equation 5. Variants of equation 5 that included time trends were also estimated, but the coefficients for the time trends were highly insignificant and had little effects on the coefficients of the other explanatory variables.

The results for selected equations for the logarithm of unit prices for EPROM's are shown in table 7. The variables have the same names as those in table 6.[13]

Equation 1 makes the logarithm of the unit price a function of the levels of density and time. Both density and time are highly significant. Equation 2 replaces density with the logarithm of density. This equation has summary statistics that are considerably higher than those in equation 1. (The level of density was never significant at the 0.9 confidence level in equations with explanatory variables in addition to time, and no additional equations with the level of density are shown.)

Equation 3 adds the two variables that proxy for life-cycle price patterns for EPROM's. The t-test statistic for the log(density) variable's coefficient decreases sharply. Equation 4 replaces the linear time trend with a logarithmic time trend and uses the level of density. In contrast to the regressions for DRAM's, the time trend is statistically significant.

Equation 5 adds the 1988–89 dummy variable that proxies for the effects of the trade agreement. While R-bar square rises slightly, to the highest value for any of the equations, the F-test statistic declines somewhat from its peak value in equation 4. The t-test statistic for density declines slightly.

The regressions yield statistically significant explanations of the prices of DRAM's and EPROM's, as measured by F-test statistics. However, the limited data available on quality characteristics that might be important to purchasers means that the regression approach is not a competitive alternative to the matched-model methodology. Aside from density and VRAM technology for DRAM's, all the other significant explanatory variables in the regressions are primarily measures of supply conditions and not of quality characteristics that affect demand. Although the importance of life-cycle variables in determining the prices of both types of memory chips is interesting, life cycles are mainly the result of supply-determining factors. Similarly, the effects of the trade agreement are not characteristics that would enter into a quality-adjusted price index.

13. There is no Stan-vram dummy variable, because this technology is not a quality characteristic for EPROM's.

Table 7.—Hedonic Regressions for EPROM's, 1976–94

[Coefficients, with t-test statistics in parentheses]

Explanatory variable	Equation number				
	1	2	3	4	5
Density	0.00034	.....	.....	0.06373	0.05863
	(7.52)	.....	.....	(1.87)	(1.74)
Log(Density)	.....	0.50381	0.6094	.....	.....
	.....	(12.16)	(1.80)	.....	.....
Time	–1.5259	–.21748	–.04164	.....	.....
	(8.87)	(13.71)	(3.12)	.....	.....
Log(Time)	.....	.....	.....	–3.68864	–3.66299
	.....	.....	.....	(3.18)	(3.20)
Nlage7max	.....	.....	0.03731	0.03697	0.03775
	.....	.....	(10.86)	(10.64)	(10.93)
Cheaprat	.....	.....	0.14048	0.14203	0.13550
	.....	.....	(4.21)	(4.27)	(4.10)
Dum8889	.....	.....	.....	.....	0.20089
	.....	.....	.....	.....	(2.00)
Constant	14.8952	18.3991	4.33743	17.1641	17.0494
	(9.97)	(14.31)	(4.03)	(3.37)	(3.39)
R-bar square	0.4575	0.6443	0.9004	0.9007	0.9032
F-test statistic	51.17	108.76	269.91	270.78	223.06
	(2,117)	(2,117)	(4,115)	(4,115)	(5,114)

NOTE.—The dependent variable is the natural logarithm of the unit price of an EPROM.
EPROM Electronically programmable read-only memory

Microprocessors

Quality-adjusted annual price indexes were estimated for two lines of MOS digital microprocessor integrated circuits; the methodology used for these indexes was quite different from that used for the indexes for memory chips. The methodology was partly based on hedonic regression equations, which were used both to construct price indexes directly and to augment the data set that was used to construct other price indexes. In addition, the methodology used conventional interpolation and extrapolation techniques that are similar to those used for some other components of the NIPA's. Although this approach echoes some aspects of the work by Roseanne Cole and her colleagues on the prices of mainframe com-

puter central processing units, it evaluates the effects of many more characteristics.[14]

After the "missing" unit prices for microprocessors were estimated, Fisher chain-type price indexes were constructed from the resulting price and quantity data using the same methodology that was used to estimate the price indexes for memory chips. Because there is no predominant univariate measure for the performance of microprocessors, an index comparable to the price indexes for the cheapest price-per-bit memory chips was not constructed.

Description of the microprocessors

The MOS digital microprocessors are key components of personal computers and include gate arrays, which are largely composed of sets of electrical circuits that carry out the three Boolean logical operations: AND, OR, and NOT. They regulate the flow of electricity according to these operations, allowing it to pass or shutting it off according to programmed instructions.[15] In addition, over time, microprocessors have increasingly added circuits that store data and instructions (in memory and registers), control other functions used to make personal computers work, and perform other operations.

Contemporary microprocessors typically have thousands, or millions, of gates and memory cells. The commands under which the microprocessors operate make up their instruction or command set, and this set varies among different types of microprocessors. Nearly all of the microprocessors included in the price index estimation are of the CISC (Complex Instruction Set Computer) variety. Of increasing importance, however, is the RISC (Reduced Instruction Set Computer) variety, which uses a more limited set of instructions to increase the speed of most operations. The technology underlying RISC microprocessors is sufficiently different that the characteristics that are important in determining the prices of CISC microprocessors may differ from those for RISC microprocessors.

Two principal lines of microprocessors are evaluated—the 80x86 line, including clones, and the 680x0 line, including follow-on PowerPC microprocessors. The 80x86-type chips have been used in IBM and IBM-compatible personal computers (PC's), and the 680x0 chips have been used in Macintosh computers. Although a number of manufacturers have produced clones of 80x86 chips, most of these chips have been produced by one manufacturer.[16]

In addition to the older generations of microprocessors, price data for Pentium microprocessors, which is an extension of the 80x86 line, are available beginning with 1993. Price data for PowerPC microprocessors are available beginning with 1995.[17] The Pentium microprocessors incorporate design improvements that yield higher performance ratings than 80486 microprocessors with the same clock speeds on many standardized tests of computing power. The RISC technology incorporated in PowerPC microprocessors also boosts performance relative to clock speed in many applications.

Distinguishing characteristics.—A number of quality characteristics can be used to measure a microprocessor's computing power, capabilities, and efficiency. The speed of operation is an important characteristic for microprocessors because it helps determine how fast the PC using the microprocessor performs. One measure of speed is the microprocessor's internal clock speed, which is measured in megahertz (millions of cycles per second). Internal clock speed is either the rate or a multiple of the rate at which the microprocessor deals with the rest of the circuits of a computer. However, clock speed does not capture all of the factors that determine the speed of a microprocessor.[18] An alternative measure of speed is MIPS (millions of instructions per second); data for this measure were available only for the 80x86 line of microprocessors, including Pentiums.

Recent microprocessors contain a number of registers that store data and instructions that are, or that are about to be, used by the logic circuits. An important characteristic is the size of the packets of information that the microprocessor's architecture allows it to deal with simultaneously; this characteristic can be measured by the "width" of the internal data registers. Some early microprocessors dealt with 8 bits simultaneously,

14. See Cole, et al., 41–50.

15. For a more complete description of microprocessors, see Rosch, 36–153.

16. This estimate is based on the commercial-source worldwide shipments data. In 1994, the principal producers of 80486-type chips, including clones, were Intel (77 percent of the total), Advanced Micro Devices (11 percent), Cyrix (5 percent), IBM (4 percent), and Texas Instruments (3 percent).

17. Manufacturers of PowerPC microprocessors include Motorola and IBM.

18. In addition to clock speed, a number of other features determine the speed of performing operations. More advanced chips typically are faster than less advanced chips with the same clock speed from the same manufacturer. For example, on a number of standard performance tests, some computers with 66-MHZ-rated Pentium microprocessors deliver much higher performance than the same manufacturer's computers with 66-MHZ-rated 80486 microprocessors; the advantages are especially large for tests using 32-bit codes. Further, the architecture of the PC helps determine its speed in performing operations. See for example, *Gateway 2000 Product Guide* (North Sioux City, SD: Gateway 2000, April 1994).

and later microprocessors deal with 16 or 32 bits.[19] Alternatively the size of the packets of information can be measured as the width of the "bus" that connects the microprocessor with the rest of the PC's circuitry. This width ranges from 8 to 64 bits and is determined by the number of parallel wires that carry data. Data for both register and bus width are available for 80x86 and 680x0 microprocessors.

A characteristic somewhat related to register width and to bus width is the amount of random access memory that the microprocessor can access at one time. The width of the "address bus" to the memory chips determines how much memory can be accessed. Generally, as register widths have increased over time, widths of address busses have also increased. The amount of memory that can be addressed is determined by the formula $M = 2^N$, where M is the number of bytes of memory that can be addressed, and N is the width of the address bus.[20]

Another characteristic that can proxy for increasing speed and capability of microprocessors is the number of transistors they contain. Data on the number of transistors were available only for 80x86 microprocessors.

Some recent types of microprocessors contain integral memory units, or "caches." These are used to temporarily hold data or instructions that are likely to be needed soon for operations by the microprocessor. Having this information on the same chip as the logic circuits helps to speed operations. The 80x86 microprocessors use one cache for both data and instructions. The first caches on 680x0 microprocessors held only instructions, but more recent types of 680x0 microprocessors have separate caches for instructions and for data.

Because general-purpose logic circuits are rather slow at doing complex mathematical operations, specialized floating-point logic units have been developed to handle them. At first, these "math coprocessors" were separate chips that worked alongside the general-purpose microprocessors. More recent types of microprocessors, however, have often included integral math coprocessors. Data on the incorporation of coprocessors are available for both 80x86 and 680x0 microprocessors.

Newer microprocessors incorporate some PC management functions that were handled by separate circuits in earlier designs. For 80x86 microprocessors, the characteristic measured was the presence of support circuits. For 680x0 microprocessors, two characteristics are measured—the presence of external memory management and, with the most recent types, the presence of integral memory management.

Some 80x86 microprocessors have the ability to multitask, or to run two or more programs at the same time. Integral multitasking capabilities were first offered on 80386 microprocessors.

In addition, the age of the types of microprocessors may be a price-determining characteristic. Alternatively, a general time trend would be indicative of price declines over time that are not related to the ages of the microprocessors.

The most recent, and capable, microprocessors incorporate additional features that speed operations; for example, "superscalar" design allows the microprocessor to do more than one operation at the same time. Such features, as well as the incorporation of RISC technology, might be expected to influence prices. However, these features are highly collinear with other characteristics and so do not appear as separate explanatory variables in the regression equations.

The prices of microprocessors may also have been influenced by such factors as the type of packaging of the chips, the operating voltage (important for notebook PC's and for some recent high-speed microprocessors), and transistor technology. However, information from the data set suggests that the price differences due to these factors are small in comparison with the effects of the other characteristics.

Clones.—Clones of 80x86 microprocessor types usually appear after the 80x86 types are introduced, and the market share of the clones gradually increases.[21] There is price data for only one clone, the AMD386 40-megahertz microprocessor.

The clones often offer a somewhat different mix of characteristics than do corresponding 80x86 microprocessors in the data set. Clones often offer somewhat greater capabilities. However, it is not unreasonable to suppose that, given the rough similarity of capabilities, the clones' prices move in the same general patterns as those of 80x86 chips included in the data set.

19. All 680x0 microprocessors in the data set have a 32-bit register width, so width is not a distinguishing characteristic for these chips. Pentium and PowerPC microprocessors incorporate some 64-bit aspects.

20. Recent types of microprocessors have additional capabilities that further enhance the speed with which they can get data to and from memory and the total amount of memory that can be addressed, but these capabilities were highly collinear with other characteristics and did not prove to be significant in the hedonic regression experiments.

21. The clones either are produced under license (for example, some IBM and Advanced Micro Devices microprocessors) or are designed to be compatible with the 80x86 microprocessors.

Data.—The microprocessor price data used in the regressions are for North American booking prices for 1985–94. Although the actual prices paid may vary somewhat from the booking prices, there is no reason to assume that they would differ consistently from the booking prices. In addition, because this analysis uses annual average prices, the effects of lags between bookings and shipments are mitigated. Research on the lags between booking prices and prices paid for memory chips (not reported here) suggests that the effects of lags are small.

Regressions for 80x86 microprocessors

The first regression-based experiments used the 80x86 microprocessor data because there were more observations and because the explanatory data set described more characteristics. The data set had a total of 72 observations available, ranging from 3 observations for 1985 to 11 observations for 1991. There were data for a total of 22 types of 80x86 microprocessors, classified by clock speed, plus the AMD386 clone. The data set did not include all speeds of a given microprocessor type in all periods, but it did include prices for more than one speed of a given microprocessor type in a given year. In many cases—for example, the 80386 series—the first year for which there were prices for a new type of microprocessor was the year following its initial introduction: The data set often indicated small numbers of shipments in the first year, but it did not include corresponding price data.

The following 12 explanatory variables were available for the regression experiments:

Speed Internal clock speed, in megahertz[22]

MIPS Computing power, in millions of instructions per second

Register Internal register width, in bits

Bus External bus width, in bits

Transistor Number of transistors on the microprocessor chip, in thousands

Memory Addressable memory, in number of bits of address register width (see previous formula)

Cache Amount of on-chip memory cache, in kilobytes

Year Year of the observation (for example, 1990 = 90)

Age Number of years since the microprocessor chip series was introduced (for example, in 1993 the age of an 80486DX chip, which was introduced in 1989, was 4)

Coprocessor Dummy variable for the existence of a math coprocessor on the microprocessor chip: Yes = 1, no = 0

Support Dummy variable for PC support/control capabilities on the microprocessor chip: Yes = 1, no = 0

Multitask Dummy variable for the ability to do multitasking on the microprocessor chip: Yes = 1, no = 0

The equations that were initially estimated focused on the key characteristics of MIPS and Speed, each in combination with time. Next, the other explanatory variables were added one at a time in the following judgmentally preferred order: Register, Bus, Transistor, Memory, Cache, Age, Coprocessor, Support, and Multitask. The variables that had t-test statistics of 1.0 or higher with either speed specification (roughly the 50-percent confidence level) were retained.

In order to avoid possible spurious results due to chance nonlinear relationships, an iterative Box-Cox test for functional form was not performed. Instead, the initial equations were estimated using four alternative functional forms: Log-log, log-linear, linear-linear, and linear-log. These four forms were also used for the second set of equations that added register width. At this point, the "preferred" equations with either speed variable had R-bar squares of about 0.9 or higher, and the log-log forms had much higher F-test statistics.[23] As a result, the log-log form was adopted for further experimentation.[24]

After a preferred equation was estimated according to the iterative process, the other explanatory variables, such as memory, that were dropped earlier were added back one at a time to see if any were significant in equations containing the preferred explanatory variables. They were not.

Table 8 shows a selected set of the log-log form equations. In equations 1 and 2, which were the starting points of the regression experiments,

22. Data on external clock speed are also available but were not used, because of high collinearity with internal clock speed.

23. For example, for the equations with MIPS, Register, and Year as explanatory variables, the F-test statistics for the various functional forms were

Log-log	308.9
Log-linear	58.8
Linear-log	54.5
Linear-linear	53.2

24. The log-log functional form was used for all but one of the nondummy explanatory variables other than Year and Age. It was not used for Cache, because Cache has a value of zero for some of the earlier microprocessor types and therefore cannot be expressed in logarithmic form.

unit prices are a function of speed and the time trend variable. Equation 1 uses MIPS as the speed measure, and equation 2 uses Speed as the speed measure. Year has a highly significant negative coefficient that is consistent with declining prices over time (this result holds for all the other equations as well). The "fits" of the equations as measured by the summary statistics are already reasonably good, and all the coefficients of the variables have highly significant t-test statistics. MIPS yields a slightly better fit than Speed.

In equations 3 and 4, which are counterparts to equations 1 and 2, Register was added as an explanatory variable. Its coefficients are positive, a result that is consistent with increased unit prices. The summary statistics improve somewhat, and the t-test statistics for each variable's coefficients are highly significant. Again, MIPS yields a slightly better fit than Speed.

Equations 5 and 6 incorporate all the nondummy measures of chip performance. The R-bar squares improve, but the F-test statistics decline somewhat, reflecting the larger number of explanatory variables. In equation 5, the coefficient of Cache is insignificant; moreover, it is negative, a result that is inconsistent with increased unit prices. Speed yields a slightly better fit than MIPS.

Equations 7 and 8 incorporate the dummy variables that describe the performance characteristics of microprocessors. All of the dummy variables' coefficients have significant t-test statistics with at least one speed variable. However, the t-test statistics for Transistor in equation 7 and for Register in equation 8 drop well below 1.0, reflecting the high degree of collinearity among the explanatory variables, including the dummy variables, in the equations.

Equations 9 and 10 add Age to the explanatory variable set. Although Age is primarily a measure of supply conditions rather than a quality characteristic affecting demand, it is included in order to look for life-cycle patterns of the prices of microprocessors that might be similar to the strong patterns found for the various types of memory chips. Adding Age roughly doubles the negative coefficient of the Year (time trend) variable; moreover, Age has a positive coefficient approximately the same size as the previous negative coefficient of the time trend. This result suggests that the prices of individual microprocessor types tend to decline more slowly over time than the quality-adjusted price of microprocessors, which also reflects the introduction of new types of microprocessors. This pattern is analogous to that of memory chips, but strong life-cycle patterns are less evident for microprocessors.

In both equations, adding Age also dramatically lowers the t-test statistics of Bus and increases the t-test statistics of both Transistor and Register.

Equation 11 is similar to equation 8, but it excludes the statistically insignificant Register variable. Equation 12 is similar to equation 10,

Table 8.—Hedonic Regressions for 80x86 Microprocessors, 1985-94

Explanatory variable	Equation number											
	1	2	3	4	5	6	7	8	9	10	11	12
Log(Speed)	.....	2.88881	.....	1.52999	.....	0.99176	.....	0.46413	.....	0.47581	0.48465	0.47740
	.....	(17.9)	.....	(6.1)	.....	(5.0)	.....	(3.0)	.....	(3.4)	(3.4)	(3.5)
Log(MIPS)	1.21178	.....	0.69201	.....	0.48408	.....	0.22524	.....	0.12350	.....	.....	.....
	(19.0)	.....	(9.1)	.....	(4.4)	.....	(2.7)	.....	(1.4)	.....	.....	.....
Log(Register)	.....	.....	2.32770	2.38626	1.75624	1.03812	0.84904	0.14523	1.44337	1.03003	.....	1.04219
	.....	.....	(8.4)	(6.3)	(5.7)	(3.1)	(2.2)	(0.4)	(3.4)	(2.5)	.....	(2.6)
Log(Bus)	.....	.....	.....	.....	0.62346	0.75728	0.32671	0.34673	0.09800	0.02410	0.34619	.....
	.....	.....	.....	.....	(2.3)	(3.0)	(1.7)	(1.9)	(0.5)	(0.1)	(1.9)	.....
Log(Transistor)	.....	.....	.....	.....	0.28486	0.46221	0.05489	0.12684	0.10362	0.14101	0.12139	0.14326
	.....	.....	.....	.....	(2.2)	(4.2)	(0.6)	(1.4)	(1.1)	(1.7)	(1.4)	(1.4)
Cache	.....	.....	.....	.....	–0.1159	0.03644	0.01099	0.05754	0.06732	0.10882	0.06358	0.10921
	.....	.....	.....	.....	(0.4)	(1.6)	(0.4)	(2.2)	(2.0)	(4.1)	(3.1)	(4.1)
Year	–0.24272	–0.33258	–0.20617	–0.23786	–0.23322	–0.30509	–0.22026	–0.25173	–0.41138	–0.49226	–0.25358	–0.49549
	(6.0)	(7.2)	(7.1)	(6.0)	(8.4)	(9.9)	(11.6)	(11.3)	(5.7)	(7.8)	(11.8)	(8.7)
Age	.....	.....	.....	.....	.....	.....	.....	.....	0.21830	0.27060	.....	0.27442
	.....	.....	.....	.....	.....	.....	.....	.....	(2.8)	(4.0)	.....	(4.6)
Coprocessor	.....	.....	.....	.....	.....	.....	1.07509	0.87492	1.09237	0.87284	0.84618	0.87214
	.....	.....	.....	.....	.....	.....	(6.2)	(4.7)	(6.6)	(5.2)	(5.0)	(5.2)
Support	.....	.....	.....	.....	.....	.....	0.76248	0.73808	1.59025	1.71035	0.73860	1.72643
	.....	.....	.....	.....	.....	.....	(5.2)	(5.0)	(4.8)	(6.2)	(5.1)	(7.1)
Multitask	.....	.....	.....	.....	.....	.....	1.42498	1.74107	2.36798	2.70367	1.82437	2.72775
	.....	.....	.....	.....	.....	.....	(4.3)	(5.7)	(5.1)	(7.5)	(9.1)	(8.8)
Constant	24.202	25.8223	14.1657	13.4625	15.2709	20.4055	17.7464	21.1432	31.1581	38.0158	21.6911	38.2782
	(6.7)	(6.7)	(5.0)	(3.7)	(5.9)	(7.0)	(9.1)	(9.3)	(6.0)	(8.2)	(12.6)	(9.2)
R-bar square	0.8565	0.8406	0.9286	0.8984	0.9410	0.9449	0.9733	0.9739	0.9759	0.9791	0.9743	0.9794
F-test statistic	212.9	188.1	308.9	210.2	189.8	203.9	289.1	295.8	288.5	333.8	337.4	376.9
	(2,69)	(2,69)	(3,68)	(3,68)	(6,65)	(6,65)	(9,62)	(9,62)	(10,61)	(10,61)	(8,63)	(8,63)

NOTE.—The dependent variable is the natural logarithm of the unit price of an 80X86 microprocessor.

but it excludes the statistically insignificant Bus variable. Excluding the insignificant variables has little effect on the coefficients of the remaining variables, and it improves the summary statistics slightly.

The equation specification that uses Speed as an explanatory variable is preferred to the one using MIPS. In addition, ratings for speed (in megahertz), but not for MIPS, are available for the 680x0 microprocessors, and it seemed advantageous to make the equations for the two lines of microprocessors as similar as possible.

Equation 11 was selected as the starting point for the final regression equation that would be the basis for the hedonic price index work. Next, dummy variables were substituted for the Year time trend for each year. As a result of this substitution, the t-test statistics for Cache and Support fell below 1.0. The time dummy variables have increasingly negative coefficients, consistent with price declines over time. The final estimated regression is

$$
\begin{aligned}
&\log(\text{Price}) = \\
&0.72368 * \log(\text{Speed}) && +0.33233 * \log(\text{Bus}) \\
&(4.7) && (1.6) \\
&+0.48027 * \log(\text{Transistor}) && +0.87170 * \text{Coprocessor} \\
&(6.2) && (5.7) \\
&+1.28774 * \text{Multitask} && -0.12929 * D86 \\
&(6.2) && (0.5) \\
&-0.23317 * D87 && -0.22704 * D88 \\
&(1.0) && (1.0) \\
&-0.50193 * D89 && -1.003384 * D90 \\
&(2.2) && (4.6) \\
&-1.22490 * D91 && -1.64202 * D92 \\
&(5.2) && (6.6) \\
&-1.97719 * D93 && -2.23826 * D94 \\
&(7.7) && (8.2) \\
&-1.56854 \\
&(1.6) \\
&\text{R-bar square} = 0.9680 \\
&F\ (14,57) = 154.4
\end{aligned}
$$

(In the equation, the variables labeled as Dyy are the time-related dummy variables; yy is the year of the observation.)

Regressions for 680x0 microprocessors

Next, experiments were conducted with the data set for 680x0 microprocessors. The data set had a total of 48 observations available, ranging from 1 observation in 1985 to 8 observations in 1990. Data were available for 8 types of 680x0 microprocessors, classified by clock speed. Like the data set for 80x86 microprocessors, this data set did not track all speeds of a given type of microprocessor in all periods, but there were a number of overlaps. For microprocessors that were introduced in 1985–94, price data were available beginning with the year after the year of introduction.

The following 10 explanatory variables were used for the regression experiments:

Speed Internal clock speed, in megahertz

Bus Bus interface width, in bits (this is similar to but not identical with the Bus measure used for 80x86 microprocessors)

Memory Addressable memory, in number of bits of address register width (see the formula for 80x86 microprocessors)

Year Year of observation (for example, 1990 = 90)

Age Number of years since the microprocessor was introduced

Dcache Number of bits of data available in cache memory, on the microprocessor chip

Icache Number of instructions that can be stored in cache memory, on the microprocessor chip

Pipeline Dummy variable for the existence of pipeline logic operations on the chip; also denotes the existence of a floating-point logic circuit on the microprocessor chip: Yes = 1, no = 0

Manage Dummy variable for the existence of an external memory-management circuit on the microprocessor chip: Yes = 1, no = 0

Manage-I Dummy variable for the existence of an internal memory-management unit on the microprocessor chip: Yes = 1, no = 0

The estimation process was largely the same as that for 80x86 microprocessors, but it used shortcuts based on the results of the 80x86 estimates. In particular, only the log-log functional form was used. Because for the 680x0 microprocessors, Memory is perfectly correlated with Bus, Memory was dropped as an explanatory variable. Because of the high correlations among the explanatory variables, the number of variables that could be included in the preferred equation was even fewer than for the 80x86 microprocessors.

Table 9 shows a selected set of equations. In equation 1, the starting point of the experiments, the unit price of the microprocessors is a function of Speed and Year. Equation 2 adds Bus to the explanatory variable set. In these equations, as well as in most of the other equations shown, the Year variable's coefficient is negative, which is consistent with the pattern of declining prices over time. As before, positive coefficients for the performance variables are consistent with the premise that additional features increase unit prices. All t-test statistics in the two equations

are highly significant, and the summary statistics are reasonably good.

Equation 3 adds Pipeline, which has a high t-test statistic and improves summary statistics. However, Pipeline is highly correlated with other explanatory variables and is never significant when any of the others are added; as a result, it is not used in any other equations in table 9.

Equations 4 and 5 add Dcache and Icache, respectively, to the explanatory variable set. The coefficient of each of the cache variables is highly significant, and each yields greater improvements to the summary statistics than Pipeline. The two cache variables have a correlation coefficient of 0.997, so it was not possible to get both of them to be significant in the same equation. Dcache turned out to be a slightly better explanatory variable, so it is used in the preferred equation.

Equation 6 adds the two memory-management circuit variables. All of the variables are highly significant, and the summary statistics are quite good. (Additional work showed that Manage is significant without the inclusion of Manage-I, but not conversely.) All of the performance variables' coefficients are positive.

Equation 7 is similar to equation 4, but it adds Age to the explanatory variable set. The coefficient of Age is negative, and it is about the same size as the coefficient of Year in the other equations. In addition, the Year coefficient becomes highly insignificant. This result is the reverse of the results for 80x86 microprocessor prices; however, it is consistent with the pattern of prices declining over time that results from price declines in prices of individual microprocessors as their designs become older.

Equation 8 drops the Year variable and adds the two memory-management variables; however, their coefficients are insignificant. The summary statistics for this equation are similar to those for equation 6.

Equation 6 was selected as the starting point for the final regression equation that would be used as the basis for the hedonic price estimates. Next, the Year time trend was replaced by individual dummy variables for each year. Unlike the corresponding equation for 80x86 microprocessors, all of the performance-characteristic explanatory variables from equation 6 were significant in the resulting equation. In addition, substituting Icache for Dcache did not affect the time dummy coefficients to 5 decimal places or the summary statistics to 4 places, but the t-test statistic for Manage-I increased 0.5, to 8.3. The estimated regression is

$$
\begin{aligned}
&\log(\text{Price}) = \\
&1.27102 * \log(\text{Speed}) && +0.97516 * \log(\text{Bus}) \\
&(5.1) && (8.3) \\
&+0.00098 * \text{Icache} && +0.89557 * \text{Manage} \\
&(8.1) && (5.8) \\
&+1.55735 * \text{Manage-I} && -0.13063 * D86 \\
&(8.3) && (0.4) \\
&-0.46500 * D87 && -0.60028 * D88 \\
&(1.4) && (1.9) \\
&-0.78569 * D89 && -1.00557 * D90 \\
&(2.5) && (3.3) \\
&-1.22273 * D91 && -1.52591 * D92 \\
&(4.0) && (4.9) \\
&-1.93050 * D93 && -2.08266 * D94 \\
&(6.2) && (6.7) \\
&-2.90252 \\
&(3.9) \\
&\text{R-bar square} = 0.9637 \\
&F\ (14,33) = 90.2
\end{aligned}
$$

Price indexes for 1985–94

The preferred hedonic equations—with year dummy variables—were used to construct two types of quality-adjusted price indexes for the 80x86 and the 680x0 microprocessors. The first type was a "regression" price index. In regression indexes, the coefficients of characteristics and of the year dummy variables are used to construct a price index. As Cole and others have noted, regression indexes are unweighted and may therefore produce different results than alternative methods.[25] The second type was a "composite" price index. Composite indexes use prices in a matched-model framework. Actual microprocessor prices are used when they are available; otherwise, hypothetical prices based on equation

25. See Cole, et al., 48–49.

Table 9.—Hedonic Regressions for 680x0 Microprocessors, 1985–94

Explanatory variable	Equation number							
	1	2	3	4	5	6	7	8
Log(Speed)	3.60632	2.24665	1.64466	1.25183	1.28761	1.33620	1.33742	1.22620
	(12.4)	(4.5)	(3.9)	(3.5)	(3.4)	(6.1)	(6.0)	(6.1)
Log(Bus)	.....	1.83498	2.23686	2.41715	2.34678	1.02843	.46449	.31417
	.....	(3.2)	(4.8)	(6.3)	(5.8)	(3.5)	(1.4)	(1.0)
Year	–0.30897	–0.27285	–0.27589	–0.25642	–0.25489	–0.24755	–0.01279	.....
	(6.1)	(5.8)	(7.3)	(8.2)	(7.7)	(12.5)	(0.4)	.....
Age	.....	.....	.....	.....	.....	.....	–0.24101	–0.24755
	.....	.....	.....	.....	.....	.....	(8.1)	(12.5)
Dcache	.....	.....	.....	0.00043	.....	0.00033	0.00019	0.00020
	.....	.....	.....	(7.6)	.....	(8.4)	(4.0)	(4.8)
Icache	.....	.....	.....	.....	0.00126	.....	.....	.....
	.....	.....	.....	.....	(6.9)	.....	.....	.....
Pipeline	.....	.....	1.46224	.....	.....	.....	.....	.....
	.....	.....	(5.0)	.....	.....	.....	.....	.....
Manage	.....	.....	.....	.....	.....	0.90321	.....	0.16057
	.....	.....	.....	.....	.....	(6.3)	.....	(1.0)
Manage-I	.....	.....	.....	.....	.....	1.48509	.....	0.03282
	.....	.....	.....	.....	.....	(8.4)	.....	(0.2)
Constant	21.7361	16.2533	16.7477	15.3848	15.3633	17.9909	1.12248	0.41510
	(5.2)	(3.9)	(5.0)	(5.6)	(5.3)	(10.3)	(0.5)	(0.7)
R-bar square	0.7641	0.8045	0.8731	0.9150	0.9057	0.9672	0.9660	0.9627
F-test statistic	77.1	65.5	81.9	127.4	113.9	231.9	267.8	231.9
	(2,45)	(3,44)	(4,43)	(4,43)	(4,43)	(6,41)	(5,42)	(6,41)

NOTE.—The dependent variable is the natural logarithm of the unit price of a 680X0 microprocessor.

values (that is, estimated prices based on the year and the microprocessor's characteristics) or on conventional interpolation and extrapolation techniques are used.

The price indexes presented in this article differ in concept from those developed by Cole and others because these indexes are chain-type indexes rather than indexes with fixed base-period weights. The chain-type-index approach for preparing composite indexes requires fewer estimated prices than approaches with base-period weights. In the calculation of the composite indexes for 80x86 microprocessors, 32 percent of the unit prices were estimates based on the final hedonic regression equation, and an additional 10 percent were extrapolated or interpolated using conventional techniques. In the calculation of the composite indexes for 680x0 microprocessors, the figures were 7 percent and 9 percent, respectively.

80x86 price indexes.—Table 10 shows four price indexes for 80x86 microprocessors for 1985–94. In 1985–94, the regression price index declines at an average annual rate of 22 percent. It declines sharply in most years but registers a small increase in 1988. The rates of decline peak at 41 percent in 1990 but continue to decline rapidly thereafter.

The other three indexes are chain-type price indexes. The Laspeyres and Paasche indexes are shown largely as background information. The Fisher index is featured in this article, as it is in the NIPA's. In 1985–94, the Fisher index declines at an average annual rate of 27 percent. It declines less in 1987 and 1988 than in the other years, but the pattern is much less emphatic than that shown in the regression index. The sharpest decline is 39 percent in 1994, and there is no apparent deceleration of the index.

680x0 price indexes.—Table 11 shows four price indexes for 680x0 microprocessors. In 1985–94, the regression price index declines at an average annual rate of 21 percent. The index declines substantially in all years, including 1988. This index shows considerably more year-to-year fluctuation than the regression index for 80x86 microprocessors. The smallest decline is 12 percent in 1986, and the largest decline is 33 percent in 1993.

The Fisher chain-type price index declines at an average annual rate of 23 percent in 1985–94. Its rate of decline exhibits considerable year-to-year volatility. The smallest decline is 15 percent in 1994, and the largest decline is 38 percent in 1993.

Extension to 1995–96

As with memory chips, price and quantity data for 1995 and 1996 became available after the regression experiments were completed. The regression experiments were not repeated with a longer sample period, because the most recently introduced microprocessors have performance-enhancing characteristics that are not in the ex-

Table 10.—Price Indexes for 80x86 Microprocessors

Year	Regression index	Chain indexes		
		Laspeyres	Paasche	Fisher
	Levels [1992=100]			
1985	5.11	6.11	9.93	7.79
1986	4.49	4.15	6.04	5.01
1987	4.05	3.77	5.38	4.50
1988	4.08	3.39	4.71	4.00
1989	3.10	2.57	3.32	2.92
1990	1.82	1.86	1.89	1.88
1991	1.50	1.54	1.56	1.55
1992	1.00	1.00	1.00	1.00
1993	0.71	0.71	0.72	0.72
1994	0.55	0.37	0.51	0.43
	Percent change from previous year			
1986	–12.1	–32.1	–39.1	–35.7
1987	–9.9	–9.1	–11.0	–10.1
1988	0.6	–10.0	–12.6	–11.3
1989	–24.0	–24.3	–29.4	–26.9
1990	–41.3	–27.5	–43.2	–35.8
1991	–17.4	–17.2	–17.1	–17.2
1992	–33.4	–35.2	–36.1	–35.6
1993	–29.2	–28.9	–27.7	–28.3
1994	–23.0	–48.0	–29.7	–39.5
Average: 1985–94	–22.0	–26.8	–28.1	–27.4

Table 11.—Price Indexes for 680x0 Microprocessors

Year	Regression index	Chain indexes		
		Laspeyres	Paasche	Fisher
	Levels [1992=1.00]			
1985	4.60	6.81	4.78	5.71
1986	4.04	5.74	3.93	4.75
1987	2.89	3.87	2.90	3.35
1988	2.52	3.14	2.53	2.82
1989	2.10	2.57	2.12	2.33
1990	1.68	1.90	1.75	1.82
1991	1.35	1.39	1.30	1.35
1992	1.00	1.00	1.00	1.00
1993	0.67	0.60	0.65	0.62
1994	0.57	0.51	0.55	0.53
	Percent change from previous year			
1986	–12.2	–15.8	–17.8	–16.8
1987	–28.4	–32.5	–26.2	–29.4
1988	–12.7	–18.8	–12.7	–15.8
1989	–16.9	–18.4	–16.4	–17.4
1990	–19.7	–26.0	–17.4	–21.8
1991	–19.5	–26.8	–25.5	–26.1
1992	–26.2	–28.0	–23.3	–25.7
1993	–33.3	–39.8	–35.2	–37.6
1994	–14.1	–15.6	–15.3	–15.4
Average: 1985–94	–20.7	–25.1	–21.4	–23.2

planatory variable set used for 1985–94.[26] Adding 2 more years of observations was not sufficient to accurately estimate the values of these characteristics. As a result, the "missing" prices—that is the prices for which 1995–96 data were not available—were estimated using conventional interpolation and extrapolation techniques.

As shown in the following tabulation, the prices of microprocessors continued to decline in 1995–96. For 80x86 microprocessors, the Fisher chain-type price index drops especially sharply, registering much larger rates of decline than those in previous years. This drop reflects very large declines in unit prices for the various types of 80486 and Pentium microprocessors. For 680x0 microprocessors, the Fisher chain-type price index declines at about the same rate in 1995 as in 1994 and then declines more rapidly in 1996. The sharp 1996 decline reflects large decreases in unit prices for the 68040 and the various PowerPC microprocessors. Thus, for both lines of microprocessors, the sharp rates of decline are associated with the newest, most technologically advanced microprocessors.

Microprocessor Price Indexes

[Percent change]

	80x86	680x0
1995	-69.8	-14.2
1996	-63.3	-32.9

Summary price index

A summary Fisher chain-type price index for both types of microprocessors was constructed using the two individual Fisher chain-type price indexes. The summary index uses current-dollar shipment weights based on unit prices and quantities of shipments from the data set. The weight for 80x86 microprocessors ranges from a low of 80 percent in 1989 to a high of 93 percent in 1994.

The summary Fisher chain-type price index for microprocessors declines at an average annual rate of 35 percent in 1985–96 (table 12). It also fluctuates considerably from year to year. The smallest decline is 12 percent in 1988, and the largest declines are 66 percent in 1995 and 60 percent in 1996. In comparison, the summary price index for memory chips declines at an average annual rate of 18 percent in the same period; the rates of change vary from a decline of 53 percent in 1985 to an increase of 16 percent in 1988.

26. Only one price observation on a Pentium microprocessor was in the data set used to estimate the hedonic regressions for the 80x86 microprocessors.

Table 12.—Summary Price Index for Microprocessors

[1992 = 1.00]

Year	Index	Percent change from previous year
1985	7.24	.....
1986	4.89	–32.4
1987	4.27	–12.8
1988	3.77	–11.8
1989	2.81	–25.4
1990	1.87	–33.3
1991	1.53	–18.5
1992	1.00	–34.5
1993	0.71	–29.1
1994	0.44	–44.2
1995	0.15	–65.6
1996	0.06	–60.1
Average: 1985–96	.....	–35.3

Semiconductor Price Indexes in the NIPA's

The price indexes for semiconductors play a modest role in the calculation of real gross domestic product (GDP). Most semiconductors are used as intermediate inputs and are netted out before the various real product-side components are calculated. However, exports and imports of semiconductors are separately identifiable components of GDP beginning with 1981. As part of the comprehensive revision of the NIPA's that was released in January 1996, the semiconductor price indexes described in this article were used in calculating real exports and imports of semiconductors. In the annual NIPA revision that was released in July 1997, these price indexes were revised and extended for use in calculating real exports and imports of semiconductors for 1993–96.

The price indexes for semiconductors play a significant role in the estimates of real gross product originating by industry. They affect both the real output of the industry in which semiconductors are produced and the real intermediate inputs of semiconductors into the industries that use them to make other products.

Exports and imports

The price indexes for exports and imports of semiconductors for 1993–96 are based on BEA's price indexes for memory chips and microprocessors and on the producer price index (PPI) for semiconductor dice and wafers. The estimates for 1981–92 are also based on BEA's price indexes, but the methodology was somewhat simpler and was based on the less complete information that was available at the time of the comprehensive revision of the NIPA's.

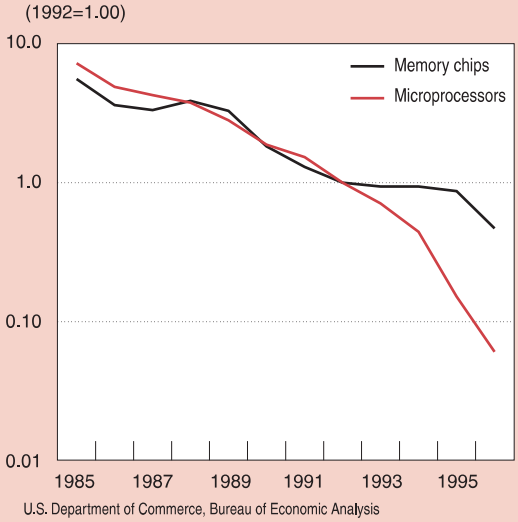
Differences between the estimates of export prices and import prices of semiconductors reflect differences in the relative importance of the two types of semiconductors in exports and imports. Microprocessors are more important than memory chips in domestic production and exports, whereas memory chips are more important than microprocessors in imports. In addition, exports include substantial numbers of domestically produced silicon wafers and semifinished semiconductor dice that are shipped abroad for further manufacturing, testing, and packaging; imports contain fewer numbers of dice and wafers.

The price weights used for exports of semiconductors are roughly as follows: One-quarter for semiconductor dice and wafers, one-third for memory chips, and the remainder—somewhat less than half—for microprocessors. The price weights used for imports of semiconductors are roughly as follows: Somewhat less than one-tenth for semiconductor dice and wafers, three-quarters for memory chips, and the remainder for microprocessors. These weighting schemes are based on the implicit assumption that the prices of other types of semiconductors follow the same patterns as the prices of the types of semiconductors used to calculate of BEA's price indexes.

In 1992–96, the price index for microprocessors, which are relatively more important in exports, declined somewhat more rapidly than the price index for memory chips, which are relatively more important in imports (chart 2). However, because of the heavier weight of semiconductor wafers and dice—whose prices have declined less rapidly than those of finished semiconductors—in the exports index, the average rates of decline in the exports and imports price indexes were about the same. Using the new price indexes raises the average annual growth rates of real exports and imports of semiconductors in 1985–94 by roughly equal amounts relative to the previous estimates.

CHART 2

Semiconductor Price Indexes



U.S. Department of Commerce, Bureau of Economic Analysis

Quarterly estimates.—Two different quarterly indicator series are used to interpolate between and extrapolate from the annual estimates for semiconductors; both series are based on price indexes published by the Bureau of Labor Statistics. For exports, the indicator series used is a weighted sum of detailed PPI's for selected semiconductors. For imports, the indicator series used is the International Price Project index for imports of semiconductors.

Gross product originating in the semiconductors industry

The price indexes described in this article were also incorporated into the gross product originating (GPO) estimates of real industry gross output and real intermediate inputs for 1977–96. For gross output, the indexes were weighted together with appropriate PPI's in order to develop a composite deflator that covered all the products of the semiconductor manufacturing industry. For intermediate inputs, the same composite deflator was used for estimating the purchases by other industries of domestically produced semiconductors. In addition, the price index for imports of semiconductors was used for imported semiconductor inputs.

In particular, the incorporation of the semiconductor price indexes directly affected the estimation of the real output of the industry that produces semiconductors, the electronic and other electric equipment industry. The real growth rates for both semiconductor output and intermediate inputs were revised up substantially, especially after 1992. In turn, both real gross output and GPO in the electronic and other electric equipment industry were revised up. In industries where GPO is calculated by double deflation and where intermediate inputs of semiconductors are significant, real GPO was revised down, but real gross output was unrevised.